Amendments to the Specification

Kindly amend paragraph [0064] as set forth below:

[0064] While visiting NSB chips that have already been visited during processing of another source, certain output links may have a weight on them. If so, the output links are ordered in such a way that the one with the least weight will have higher priority for next selection. If two links have the same weight, then the one link with the smaller port identifier will get the higher priority. It can be easily seen that the output links on board from a source switch chip will be used in cyclic order while implementing the technique of the present invention, thereby satisfying the fanning condition. The same is true of the second stage of switch chips on the NSBs. While processing the NSB chips on the destination side, prioritizing does not have any ~~affect~~ effect other than reaching the destinations in some order. This is because the route to a particular destination from the middle of the network does not have any choice of paths.